

(19)



JAPANESE PATENT OFFICE

**BEST AVAILABLE COPY**

**PATENT ABSTRACTS OF JAPAN**

(11) Publication number: **08286999 A**

(43) Date of publication of application: **01 . 11 . 96**

(51) Int. Cl.

**G06F 13/16  
G06F 15/78**

(21) Application number: **07093475**

(71) Applicant: **HITACHI LTD**

(22) Date of filing: **19 . 04 . 95**

(72) Inventor: **MITSUISHI NAOMIKI**

(54) **SEMICONDUCTOR INTEGRATED CIRCUIT  
DEVICE AND COMPUTER SYSTEM USING THE  
SAME**

(57) Abstract:

**PURPOSE:** To provide a semiconductor integrated circuit device which can execute data transfer by the use of a data transfer device or a data transfer control device in parallel with processing by a data processor while minimizing the deterioration of the processing performance of the data processor by a CPU.

**CONSTITUTION:** This computer system is a microcomputer constituted of functional blocks such as the CPU, a DTC, a ROM, a RAMI, a RAMP, a timer as an I/O, a pulse output circuit, an SCI, an A/D and IOPs 1 to 11, an interruption controller, and a BSC, etc., and an internal address bus IAB and a data bus IDB are connected to the CPU, the ROM, the RAMI and the BSC, and the internal address bus PAB and the data bus PDB are connected to the BSC, the RAMP, the I/O, and the interruption controller, and in the case where the IAB, the IDB and the PAB, the PDB are not connected by the BSC, the read/write of the ROM by the CPU and the data transfer between the RAMP and the I/O by the DTC are executed in parallel.

**COPYRIGHT: (C)1996,JPO**

## BEST AVAILABLE COPY

2/5 - (C) WPI / DERWENT  
AN - 1997-025969 [03]  
AP - JP19950093475 19950419  
PR - JP19950093475 19950419  
TI - Computer system equipped with semiconductor IC device for parallel data transfer and data processing function - carries out parallel data transfer between second memory unit and data input/output unit by data transfer appts using second bus  
IW - COMPUTER SYSTEM EQUIP SEMICONDUCTOR IC DEVICE PARALLEL DATA TRANSFER DATA PROCESS FUNCTION CARRY PARALLEL DATA TRANSFER SECOND MEMORY UNIT DATA INPUT OUTPUT UNIT DATA TRANSFER APPARATUS SECOND BUS  
PA - (HITA ) HITACHI LTD  
PN → JP8286999 A 19961101 DW199703 G06F13/16 025pp  
ORD - 1996-11-01  
IC - G06F13/16 ; G06F15/78  
FS - EPI  
DC - T01  
AB - J08286999 The system consists of a data processor (CPU), a data transfer appts (DTC), a bus control unit (BSC) and a data input/output unit (I/O). The data processor, bus control unit and the first memory unit are mutually connected by a first bus (IAB). The data transfer appts, bus control unit, a second memory unit and data input/output unit are mutually connected by a second bus (PAB).  
- The bus control unit carries out control operation of the multiple bus. The first bus is used for carrying out read-out or write-in operation of data. Parallel data transfer between second memory unit and data input/output unit is carried out by the data transfer appts using the second bus.  
- ADVANTAGE - Improves processing speed of semiconductor IC. Enables increase of operating frequency simultaneously. Avoids increase in physical circuitry of microcomputer.  
- (Dwg.1/18)